ES8316

Low Power Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- 256/384Fs and USB 12/24 MHz system clocks
- Sophisticated analog input and output routing, mixing and gain
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 92 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Mic bias
- Support digital mic

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 93 dB signal to noise ratio, -85 dB THD+N
- Ground centered headphone driver
- 3-band PEQ
- Stereo enhancement
- Headphone and external mic detection
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

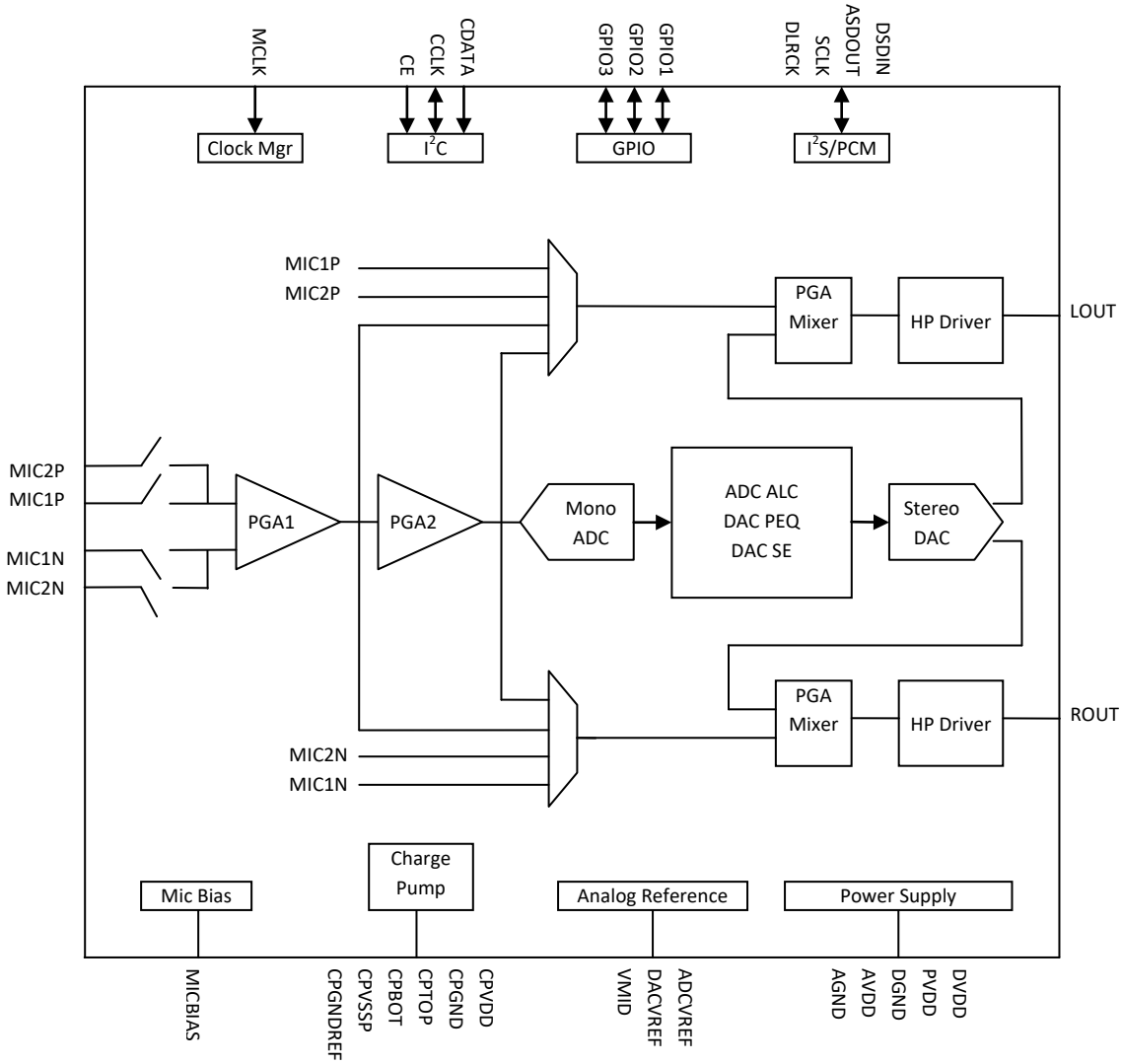
APPLICATIONS

- MID/Tablet
- Wireless audio
- Portable audio

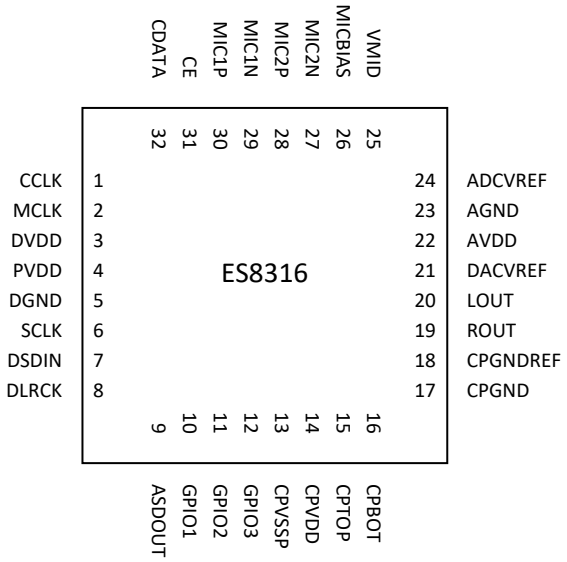
ORDERING INFORMATION

ES8316 -40°C ~ +85°C
QFN-32

1. BLOCK DIAGRAM

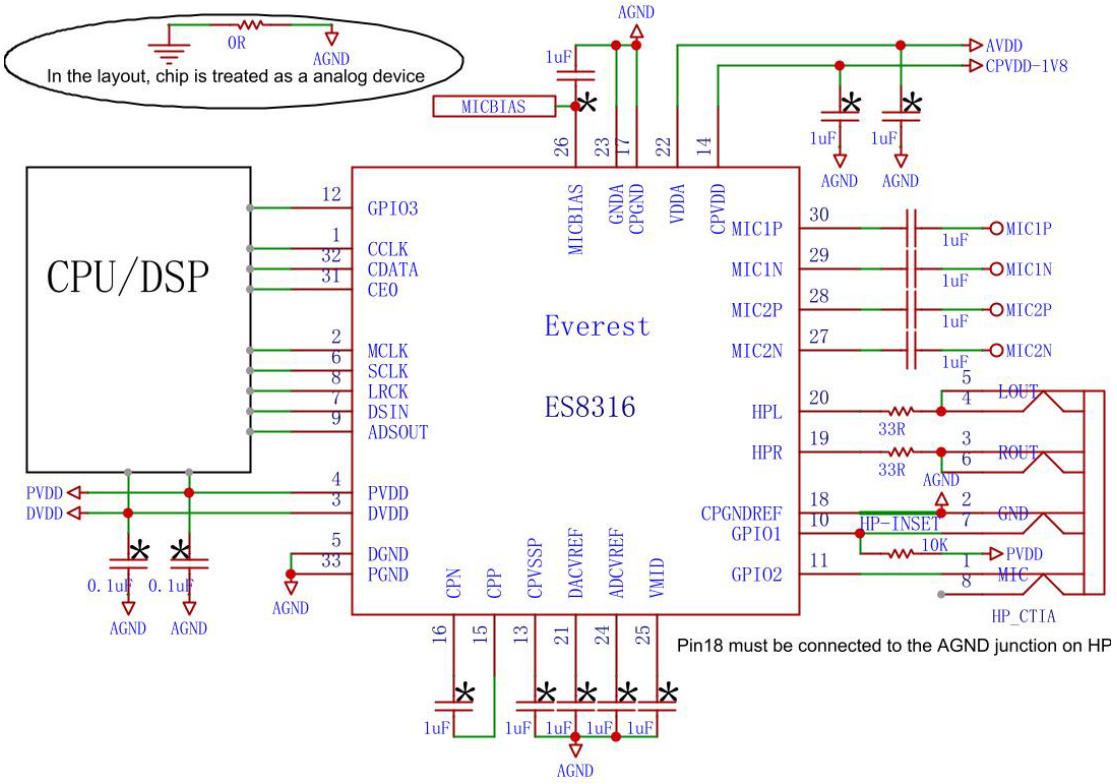


2. PIN OUT AND DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	CCLK	I	I^2C clock input
2	MCLK	I	Master clock
3	DVDD	Supply	Digital core supply
4	PVDD	Supply	Digital IO supply
5	DGND	Supply	Digital ground
6	SCLK	I/O	Audio data bit clock
7	DSDIN	I	DAC audio data
8	DLRCK	I/O	DAC audio data left and right clock
9	ASDOUT	O	ADC audio data
10	GPIO1	I/O	General purpose IO
11	GPIO2	I/O	General purpose IO
12	GPIO3	I/O	General purpose IO
13	CPVSSP		Charge pump filtering
14	CPVDD		Charge pump power supply
15	CPTOP		Charge pump capacitor top
16	CPBOT		Charge pump capacitor bottom
17	CPGND		Charge pump ground
18	CPGNDREF		Charge pump reference ground
19	ROUT	O	Right analog output
20	LOUT	O	Left analog output
21	DACVREF	O	Decoupling capacitor
22	AVDD	Supply	Analog supply
23	AGND	Supply	Analog ground
24	ADCVREF	O	Decoupling capacitor
25	VMID	O	Decoupling capacitor
26	MICBIAS	O	Mic bias
27	MIC2N	I	N analog input
28	MIC2P	I	P analog input
29	MIC1N	I	N analog input
30	MIC1P	I	P analog input
31	CE	I	I^2C device address selection
32	CDATA	I/O	I^2C data input or output

3. TYPICAL APPLICATION CIRCUIT



*For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible

4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports two types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), and USB clocks (12/24 MHz).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

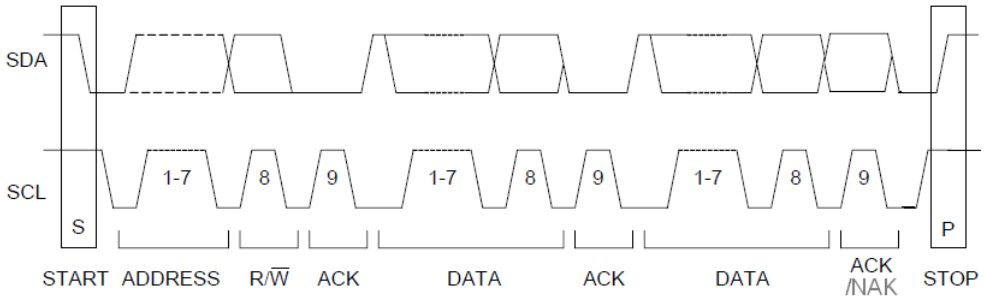


Figure 1 Data Transfer for I^2C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I²S, left justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

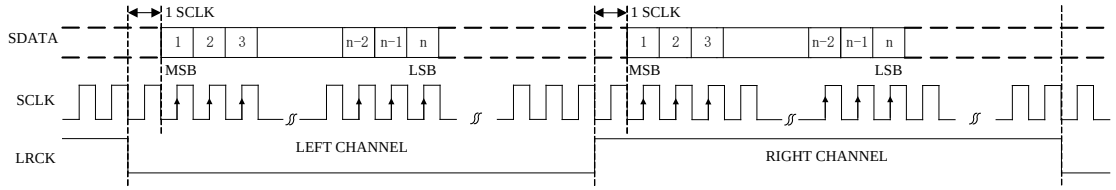


Figure 2 I²S Serial Audio Data Format Up To 24-bit

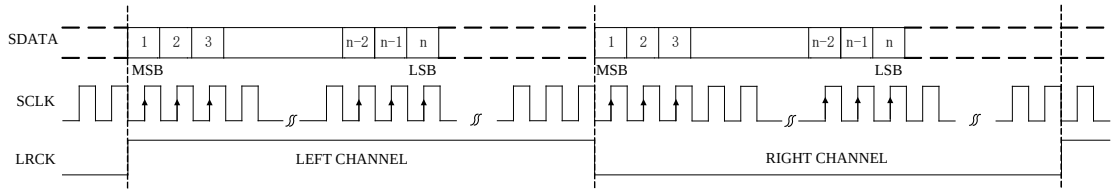


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

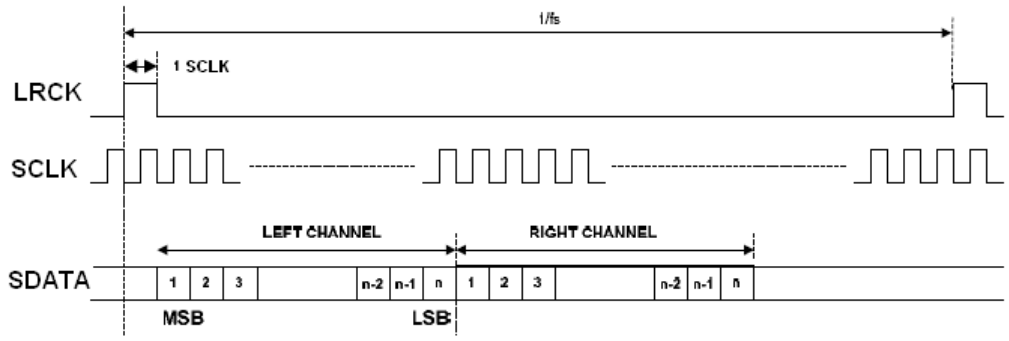


Figure 5 DSP/PCM Mode A

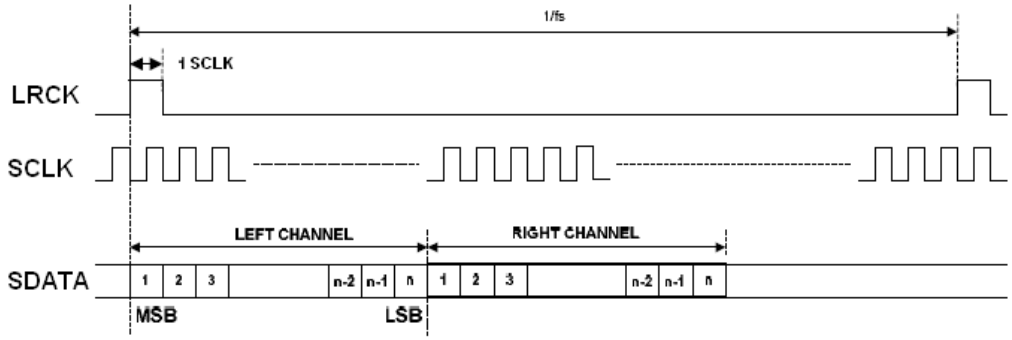


Figure 6 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	2.0	3.3	3.6	V
CPVDD	1.6	1.8	2.0	V
DVDD	1.6	1.8/3.3	3.6	V
PVDD	1.6	1.8/3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	85	92	95	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input (differential P and N)		AVDD/3.3		Vrms
Input Impedance		20		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	83	93	95	dB
THD+N	-85	-83	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	40			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB

Stopband Attenuation	40			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz Fs = 44.1KHz Fs = 48KHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		0.88*AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V: Play back Play back and record DVDD=3.3V, PVDD=3.3V, AVDD=3.3V: Play back Play back and record		 7 16 31 59		mW
Power Down Mode				
DVDD=1.8V, PVDD=1.8V, AVDD=1.8V DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		TBD TBD		mW
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

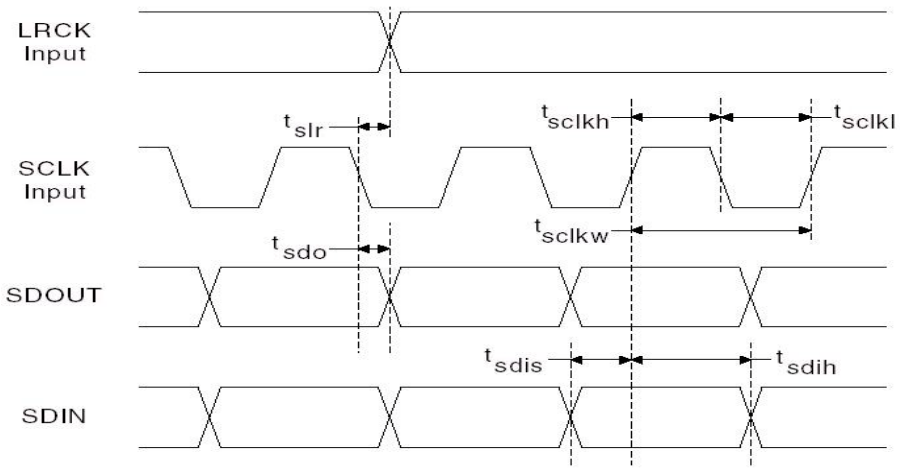


Figure 8 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

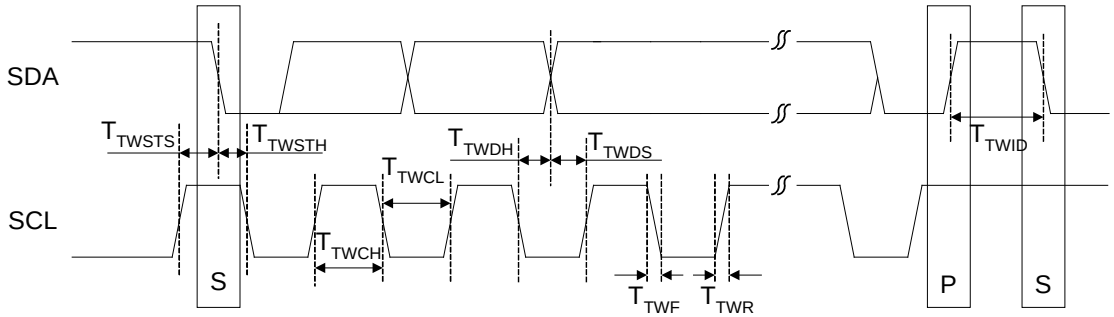
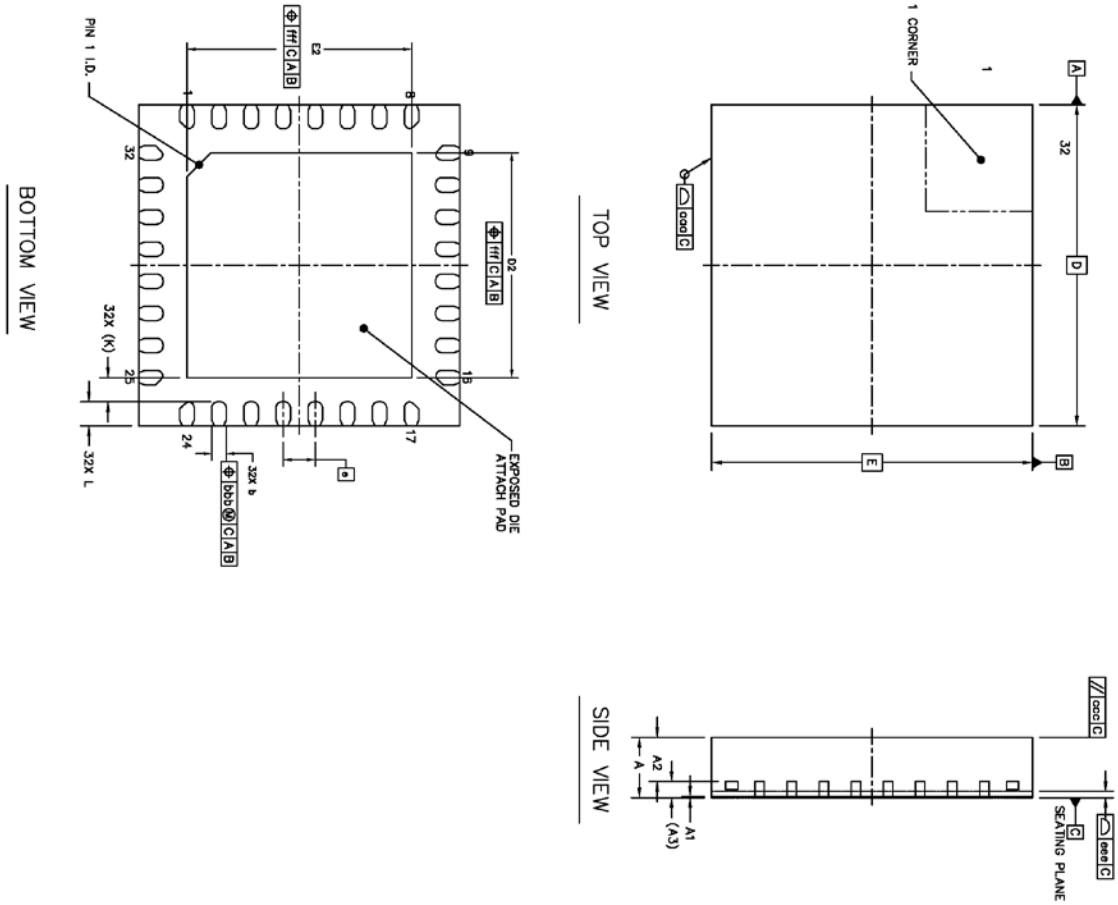


Figure 10 I²C Timing

8. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	2.7	2.8	2.9
EP SIZE Y	E2	2.7	2.8	2.9
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.3 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

9. CORPORATE INFORMATION

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